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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/726,663

11/30/2000

Chrong-Jung Lin

TS98-338B

1676

28112

7590

05/05/2004

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EXAMINER

DICKEY, THOMAS L

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/726,663

Applicant(s)

LIN ET AL.

Examiner

Thomas L Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5 and 6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3 is/are allowed.
- 6) ☒ Claim(s) 1,2,5 and 6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 17 March 2004 is: a) ☐ approved b) ☒ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

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DETAILED ACTION

1. The amendment filed on 03/17/2004 has been entered.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 03/17/04, has not been approved. These drawings add new matter not previously found in the application as filed. It appears applicant did not intend these drawings to be filed but rather to be used as a visual aid in illustrating an argument.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by CHOI et al. (5,859,454).

Choi et al. discloses a stacked-gate flash memory cell comprising a semiconductor substrate 40 having an active area (seen directly below floating Poly-Si gate 21) containing a channel region 25, a floating Poly-Si gate 21 with a bottom surface and a multiply connected top surface, the bottom surface being flat and overlying the channel

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region 25 in the active area, the multiply connected top surface overlying the bottom surface and the channel region 25; the multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of the multiply connected top surface overlying the channel region 25 in the active area is greater than the area of the bottom surface, wherein the individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes (in this case, rectangular) and the multiply connected top surface comprises five (which is more than three) individually connected top surfaces, a conformal inter-poly dielectric layer 42 replicating the individual cross-sectional shapes over the floating Poly-Si gate 21; and a conformal Poly-Si control gate 33 replicating the individual cross-sectional shapes over the inter-poly dielectric layer 42. Note figures 3A and 6 and column 6 lines 1-15 and column 7 lines 55-68 of Choi et al. Note that claim 1 places limitations on a cross-section (not, for example, all cross-sections) of a floating gate, that the floating gate 21 of Choi et al. has at least two cross-sections (two are displayed, one in figure 5 and another in figure 6) and that although the cross-section shown in figure 5 does not meet claim 1, the cross-section shown in figure 6 does in fact meet claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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Claims 2,5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over CHOI et al. (5,859,454) in view of MURAI (5,243,559).

Choi et al. discloses a stacked-gate flash memory cell with all the limitations of claims 2,5, and 6 (including an ONO inter-poly dielectric layer 42, note column 7 lines 33-37) except certain specific dimensions for the thickness of the floating gate (190-210 nm), ONO inter-poly dielectric layer (15-25 nm), and control gate (150-200 nm) Note figure 6 of Choi et al. Choi et al. is silent on the question of what these dimensions should be. However, Murai, which was published well before Choi et al. was applied for, and would have been well known to the Choi et al. inventors, discloses a stacked-gate flash memory cell with a floating gate 36 having a thickness in the range of 190-210 nm, an ONO inter-poly dielectric layer 37 having a thickness in the range of 15-25 nm, and a control gate 38 having a thickness in the range of 150-200 nm. Note column 4 lines 37, 43, and 50 of Murai. Therefore, it would have been obvious to a person having skill in the art to build a physical realization of Choi et al.'s stacked-gate flash memory cell using the dimensions taught by Murai in order to build Choi et al.'s stacked-gate flash memory cell with a minimum of experimentation. In the absence of specific instructions from Choi et al. one having skill in the art would reasonably believe that any dimensions known to Choi et al. (such as the Murai dimensions) would work.

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Response to Arguments

5. Applicant's arguments with respect to claims 1,2,5,and 6 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

6. Claim 3 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of individual shapes comprising: a semiconductor substrate having an active area; a floating Poly-Si gate with a bottom surface and a multiply connected top surface; said bottom surface being flat and overlying said active area; said multiply connected top surface overlying said bottom surface; said multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of said multiply connected top surface overlying said active area is greater than the area of said bottom surface; wherein said individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes; a conformal inter-poly dielectric layer replicating said individual cross-sectional shapes over said floating Poly-Si gate; and a conformal Poly-Si control gate replicating said individual cross-sectional shapes over said inter-poly dielectric layer, wherein said regions of individual cross-sectional shapes have a depth between about 900 to 1000 Å.

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Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

tld
04/2004


Minhloan Tran
Primary Examiner
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